

# Hardware Managers with File System Support for Faster Dynamic Partial Reconfiguration – ISPA'14

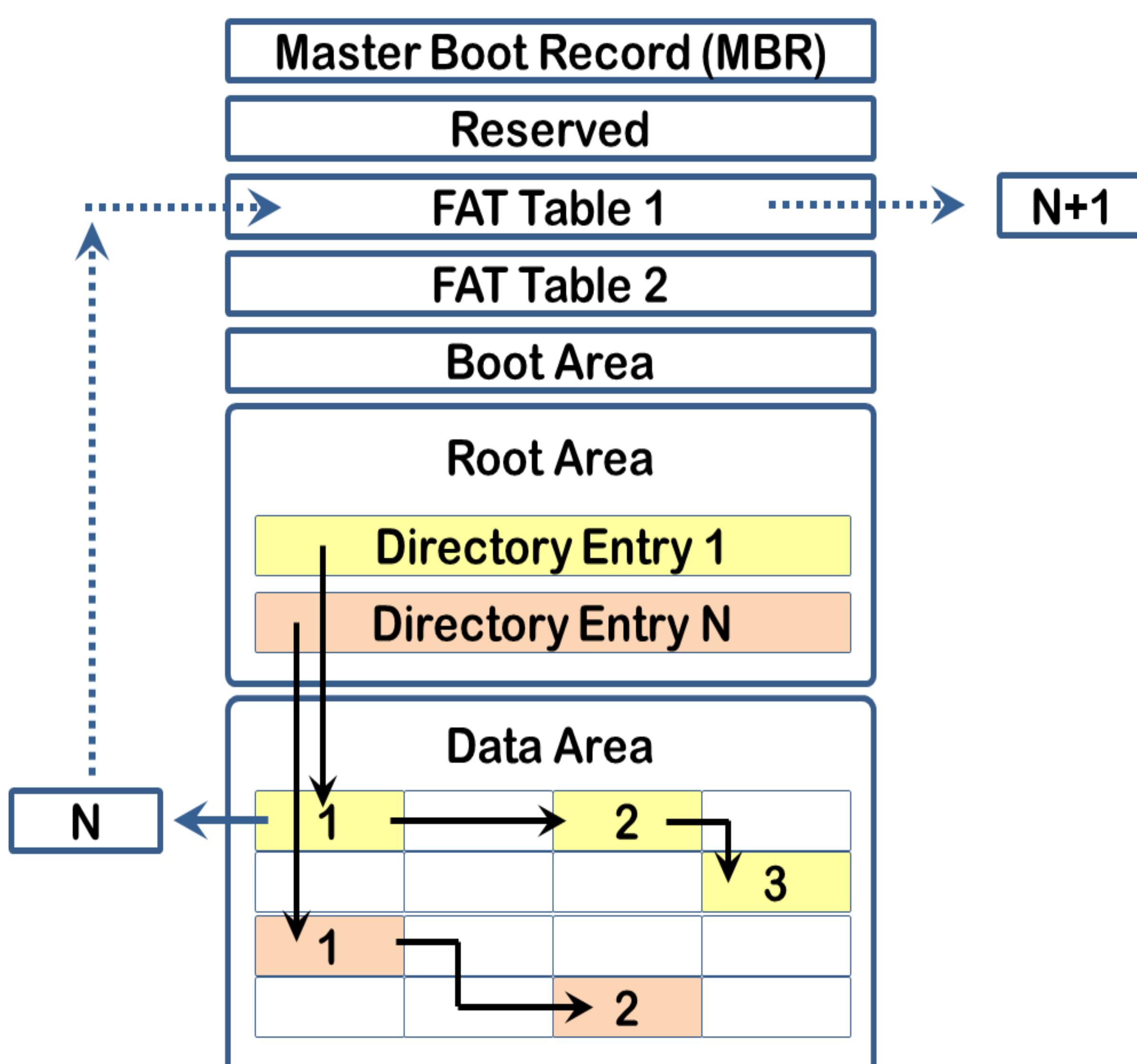
## Introduction

- Memory access is a bottleneck in HPC systems.
- DPR is a useful technique for hardware re-use that changes system functionality at runtime.
- Bitstreams are needed for DPR and are usually stored in non-volatile media which is slow in embedded systems.
- Our contribution:**
  - A hardware file system library to read FAT16 files requested by a simple command interface.
  - A rapid DPR manager without the need for a control processor.
  - Three versions of the DPR manager including controllable by a processor.

## FAT16 File System

### Device Layout

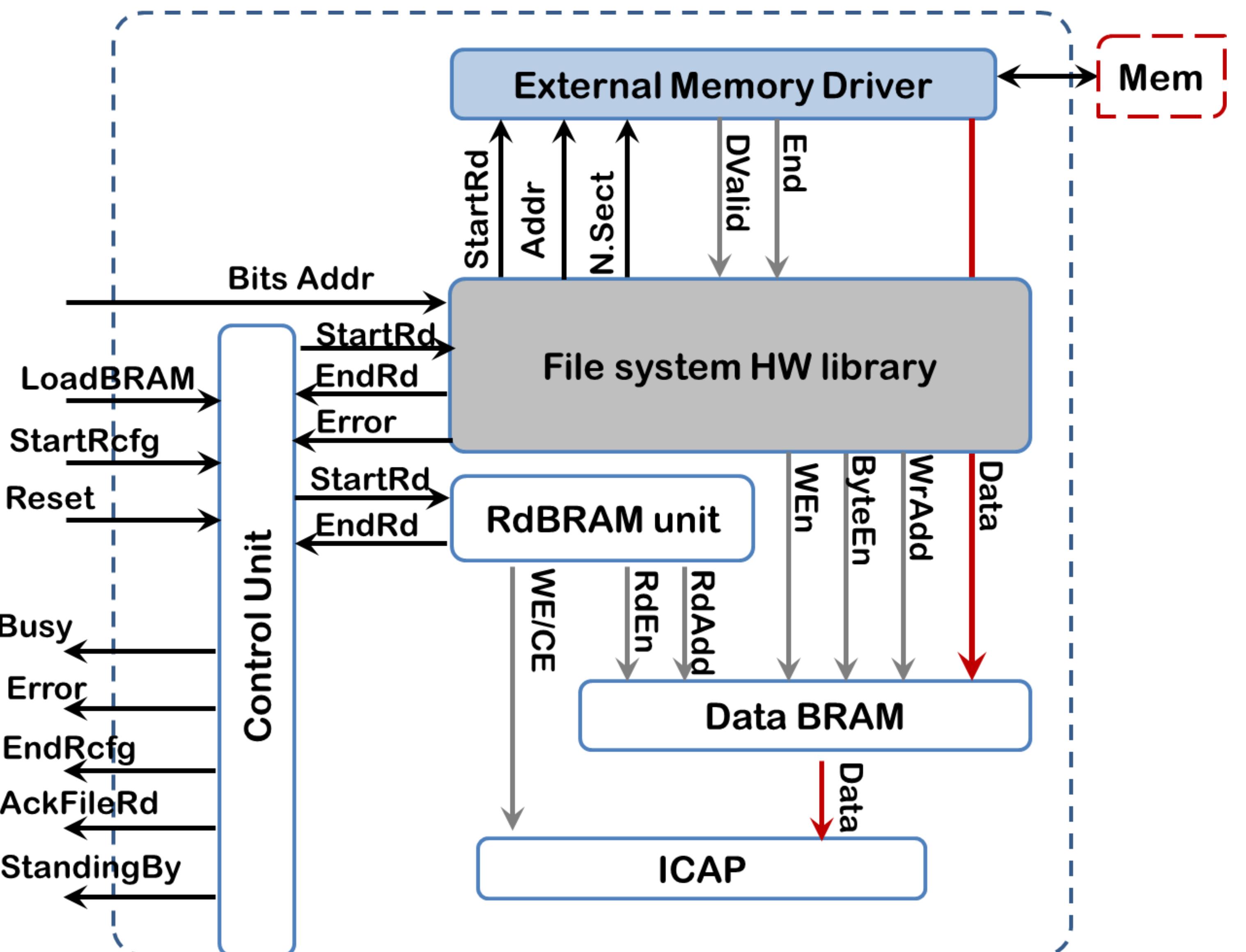
- Divided in 512Bytes/sector.
- Accessed with physical and logical addresses.
- Composed by different areas to organize files and keep device characteristics.
- Addressed by cluster number. Cluster size depends on media size or formatting options.



### Relevant area information

- MBR: Partition addresses.
- Boot area: Num. reserved sectors, FAT tables, sectors per cluster, N FAT tables, sectors per FAT table.
- Root Area Entries: File name, extension, size and cluster address.
- Files are accessed using the previous information and file system standard equations.

## Reconfiguration Manager Structure



- Simple controller interface.
- BRAM used to buffer bitstreams.
- File system HW library implements the FAT16 protocol.
- Non-portable driver for external memory.
- IP version 1: No CPU required, strict file name and with increasing index.
- IP version 2: CPU required, arbitrary file name, memory mapped.
- IP version 3: Similar to version 2 with vendor driver for memory r/w.

## Results

TABLE IV: Module comparison with most relevant State of the Art proposals

Proposal - Year	FPGA Resources			Performance		Features		Test Device	Buffering	Control Interface*
	Regs	LUTs	BRAM	Freq [MHz]	Config. Speed [MB/s]	File System	Bitstream Limit			
Lai et al. - 2009 [14]	177	303	0	90	180	N	No <sup>a</sup>	Virtex-4	SDRAM	SW/HW
Liu et al. - 2009 [11]	963	469	32	N.R <sup>b</sup>	371.4	N	64KBs	Virtex-4	BRAM	SW
Liu et al. - 2010 [22]	367	336	0	N.R	392.74	N	No	Virtex-4	SDRAM	SW
Duhem et al. - 2011 [23]	N.R	N.R	N.R	125	800 <sup>c</sup>	N	No	Virtex-5	SDRAM	SW
Vipin et al. - 2012 [24]	672	586	8	200	399.80	N	No	Virtex-6	SDRAM	SW/HW
Ours Ver-1. - 2014	378	733	16 <sup>d</sup>	116	398.6	Y	64KB <sup>e</sup>	Virtex-6	BRAM	SW/HW
Ours Ver-2. - 2014	378	781	16 <sup>d</sup>	116	398.6	Y	64KB <sup>e</sup>	Virtex-6	BRAM	SW
Ours Ver-3. - 2014	378	799	16 <sup>d</sup>	116	398.6	Y	64KB <sup>e</sup>	Virtex-6	BRAM	SW

\* Control interface is SW when a processor is required. HW/SW when IP can be used without one.

<sup>a</sup> Bitstream size limit depends on external SDRAM capacity which is always larger than any bitstream.

<sup>b</sup> N.R: Not reported.

<sup>c</sup> Obtained by overclocking the ICAP processor. Xilinx does not guarantee correct behaviour above 400 MB/s.

<sup>d</sup> User configurable parameter. More BRAM provides bigger storage.

<sup>e</sup> Value provided for test case. Absolute limit depends on FPGA BRAM capacity.

## Conclusion

- Easy to use configuration manager to handle DPR from non-CPU systems.
- Fully tested Hardware IP that implements the FAT16 protocol to read files on BRAM.
- Module extensible to FAT32/extFAT protocols.
- Close to highest vendor-suggested speed for DPR technology.